Alleviating Register Pressure for Stencil Computations

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Abstract

Register allocation is generally considered a practically solved problem. For most applications, the register allocation strategies in production compilers are very effective in controlling the number of loads/stores and register spills. However, existing register allocation strategies are not effective and result in excessive register spilling for computation patterns with a high degree of many-to-many data reuse, e.g., high-order stencils. While current state-of-the-art register allocators are satisfactory for most applications, they are unable to effectively manage register pressure for complex high-order stencils, resulting in sub-optimal code with a large number of register spills.

In this paper, we present a statement reordering framework that models stencil computations as a DAG of trees with shared leaves, and adapts an optimal scheduling algorithm to minimizing register usage for expression trees. The effectiveness of the approach is demonstrated through experimental results on a variety of stencils.