Automatic Kernel Code Generation for Focal-plane Sensor-Processor Devices

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Focal-plane sensor-processor (FPSP) devices are novel sensing-processing devices with parallel Single Instruction Multiple Data (SIMD) computational capabilities built into every pixel. FPSP devices are capable to operate at effectively very high-frame rates (around 10,000 frames per second), while consuming a fraction of the energy needed by traditional imaging devices.

FPSP devices have been used in several applications, such as real-time high dynamic range (HDR) imaging, four degrees-of-freedom visual odometry, and joint estimation of visual quantities such as optical flow and image gradient on the chip. These can play a useful part in robust navigation at high-speed camera motion, typical in autonomous cars and drones. However, progress with higher level computer vision algorithms, such as map estimation, object detection, and image segmentation, has been restricted by the limitations of these devices' hardware.

We present a code generator for filtering applications for an implementation of FPSP, known as SCAMP-5C [1]. The code generator takes the filtering kernel as input and outputs the instructions needed to implement the filtering on the chip. The SCAMP-5C chip is based on analogue technology – variables are stored as charges - and has limited memory and instructions. Each processor in the 256x256 array a photodiode sensor, but very few registers. There is no multiplication operator, and division is restricted to only powers of two. Consequently, the convolution filter implementation needs to approximate multiplication by filter kernel weights using a sequence of additions and division-by-two steps. This leads to a large number of intermediate terms that are common to different weights. The code generator produces an optimized pattern of computation and data movement that exploits these common subexpressions.

The proposed code generation algorithm has been evaluated for run-time speed and energy consumption on several convolution filters such as Gaussian kernels, Laplacian kernels, and box filters. Additionally, application of the proposed code generator is illustrated with an implementation of a Viola-Jones face detection algorithm. The results demonstrated that FPSP can achieve kernel convolution at high accuracy while (for example for the Sobel filter) consuming energy approximately 1/200th of Intel i7-3720 or 1/1000th of an NVIDIA Titan X GPU.

This talk will be based on [2] and our forthcoming paper on the topic.

[1] Stephen J Carey, Alexey Lopich, and Piotr Dudek. 2011. A processor element for a mixed signal cellular processor array vision chip. In Circuits and Systems (ISCAS), 2011 IEEE International Symposium on. IEEE, 1564–1567.

[2] Debrunner, Thomas, Automatic Code Generation and Pose Estimation on Cellular Processor Arrays. MSc Thesis, Imperial College London (2017). http://www.imperial.ac.uk/media/imperial-college/faculty-of-engineering/computing/public/student-projects-pg-2016-17/DebrunnerT-Automatic-Code-Generation-and-Pose-Estimation-on-Cellular-Processor-Arrays.pdf